Parameter Estimation for Column Level Single Slope ADC Comparators

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***Abstract*— In this paper we describe how to extract key performance parameters for the typical comparator used in a column parallel single slope ADC. We present a modified version of a comparator model. This model enables us to estimate the comparator time constant and the gain of the first stage trans-conductance amplifier. We use the measured delay time of the comparator as a function of the ramp slope. Using this model, we derive estimators for the switching speed and noise of the comparator. We also show that these estimators are in close agreement with SPICE simulation. Finally, we compare SPICE simulated noise with our model.**

I. Introduction

Column level single slope ADCs are standard circuitry for most commercial CMOS image sensors. Their performance is critical to power, readout speed, linear full well capacity and noise. Being able to model and measure their characteristics is critical to optimizing the performance of CMOS image sensors (CIS). Typically column level ADCs consist of a comparator and either a digital counter or a latch. The comparator limits the ADC speed and noise performance. Figure 1 shows standard comparator topology. The comparator consists of a five-transistor trans-conductance amplifier at the input and a two-transistor CMOS voltage amplifier at the output. Although there have been multiple papers analyzing the performance of simple comparators [1,2,3] none of these models can be used to estimate the comparator switching time and noise from measured data. The comparator time constant is critical for understanding the switching speed of the ADC and for determining the lower bound on the readout noise. Since the trans-conductance amplifier is a time varying system, where the noise is never in steady state, the noise is sensitive to the system time constant and the exact moment when the comparator switches.

The remainder of the paper is organized as follows, in Section II we present a modified comparator model and in Section III we analyze this model and derive estimators for the model parameters. In Section IV we present comparisons between the model and SPICE simulations. In Section V we discuss the limitations of the model and finally in Section VI we present summary conclusions.

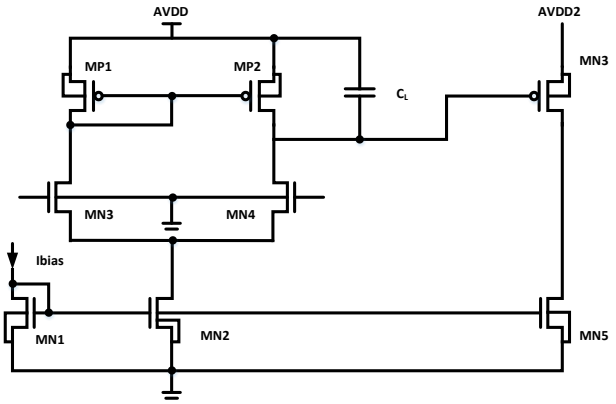

Figure 1: Standard Comparator Topology

II. Comparator Model

In Figure 2 we show a simplified model for a column parallel single slope ADC comparator. This model allows us to estimate the comparator time constant and the first stage trans-conductance amplifier gain from measured data. Note that this model flips the polarity of the comparator output in regards to the circuit shown in Figure 1. We use the measured delay time of the comparator as a function of the ramp slope to estimate its gain and time constant. The key difference in our model is that the output of the first stage trans-conductance amplifier starts to change before the inputs of the comparator are equal as shown in Figure 3. In Figure 3 K is the slope of the input ramp voltage V_{ramp}, i.e. $K = \frac{dV_{diff}(t)}{dt}$, and $t0(K)$ is the time between $V_{diff}(t) = 0$ and when the comparator output switches.

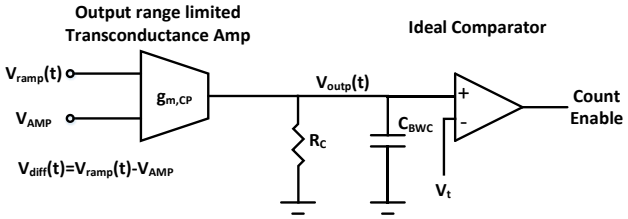

Figure 2: Comparator Circuit Model

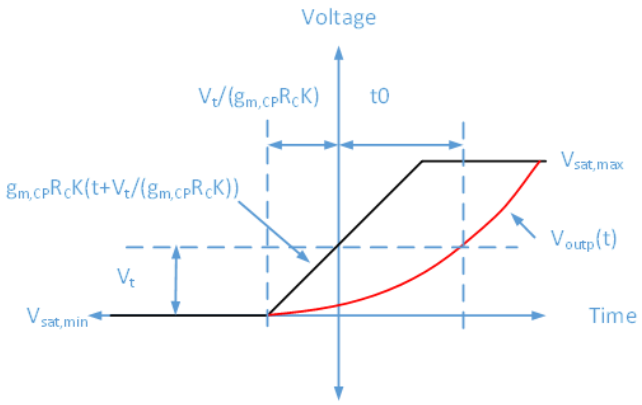

Figure 3: Model Output Waveform

The output voltage of the trans-conductance amplifier $V_{outp}(t)$ as a function of time is given by equation (1). $I_{noise,CP}(t)$ is the output referred noise current of the trans-conductance amplifier. Assuming the two sided noise power spectrum of $I_{noise,CP}(t)$ is $S_{I_{noise.CP}}(f) = 4\gamma kTg_{m,CP}$, we can transform equation (1) into an Ito form stochastic differential equation [4] as shown in equation (2). In equation (2) $\gamma = \frac{2}{3}\left(1 + \frac{g_{m,p}}{g_{m,CP}}\right)$, where $g_{m,p}$ is the trans-conductance of MP3 and $g_{m,CP}$ is the trans-conductance of MN4. Equation (2) is an Ornstein Uhlenbeck process [5] and the solutions of the mean and variance as a function of time are shown in equations (3) and (4). Using equations (5), (6) and (7) we can derive the input referred noise of the comparator as shown in equation (8).

$$V_{outp}(t) = R_C\left(\frac{dV_{diff}(t)}{dt}g_{m,CP}\left(t + \frac{V_t}{g_{m,CP}R_C\frac{dV_{diff}(t)}{dt}}\right) + I_{noise,CP}(t)\right) - R_CC_{BWC}\frac{dV_{outp}(t)}{dt} \quad (1)$$

$$dV_{outp}(t) = \left(-\frac{V_{outp}(t)}{R_CC_{BWC}} + \frac{Kg_m\left(t + \frac{V_t}{g_{m,CP}R_CK}\right)}{C_{BWC}}\right)dt + \frac{\sqrt{4\gamma kTg_{m,CP}}}{C_{BWC}}dW_t \quad (2)$$

$$E\left[V_{outp}(t)\right] = \mu_{V_{outp}}(t) = g_{m,CP}R_CK\left(\begin{array}{l}\left(t + \frac{V_t}{g_{m,CP}R_CK}\right) + \\ R_CC_{BWC}\left(e^{-\frac{(t+V_t/(g_{m,CP}R_CK))}{R_CC_{BWC}}} - 1\right)\end{array}\right) \quad (3)$$

$$Var\left[V_{outp}(t)\right] = \sigma^2_{V_{outp}}(t) = \frac{2\gamma kT}{C_{BWC}}g_{m,CP}R_C\left(1 - e^{-\frac{2(t+V_t/(g_{m,CP}R_CK))}{R_CC_{BWC}}}\right) \quad (4)$$

$$\frac{d\mu_{V_{outp}}(t)}{dt} = A_vK\left(1 - e^{-\frac{(t+V_t/(A_vK))}{R_CC_{BWC}}}\right) \quad (5)$$

$$\frac{d\mu_{V_{outp}}(t)}{dv_{diff}} = \frac{d\mu_{V_{outp}}(t)}{dt}\frac{dt}{dv_{diff}} = \left(A_vK\left(1 - e^{-\frac{(t0+v_t/(A_vK))}{r_CC_{BWC}}}\right)\right)\frac{1}{K} \quad (6)$$

$$Var\left[V_{diff}(t)\right] = \sigma^2_{V_{diff}}(t) = \sigma^2_{V_{outp}}(t)\left(\frac{dV_{diff}(t)}{d\mu_{V_{outp}}(t)}\right)^2 \quad (7)$$

$$\sigma^2_{V_{diff}}(t) = \frac{2\gamma kT}{C_{BWC}A_v}\frac{\left(1 - e^{-\frac{2(t+V_t/(A_vK))}{R_CC_{BWC}}}\right)}{\left(1 - e^{-\frac{(t+V_t/(A_vK))}{R_CC_{BWC}}}\right)^2} \quad (8)$$

We evaluate equation (8) at $t = t0(K)$, the switching time of the comparator, to estimate the lower bound on the input referred noise.

III. Model Analysis

In this Section we estimate all of the model parameters. Using equation (3) we can calculate the comparator time constant R_CC_{BWC}. In our model, the output of the comparator switches when the voltage of the trans-conductance amplifier is greater than or equal to V_t. Therefore we evaluate equation (3) when $V_{outp}(t0(K)) = V_t$ as shown in equation (9). Note that the comparator voltage gain $A_v = R_Cg_{m,CP}$. Assuming that $R_CC_{BWC} \gg t0(K)$ and using a second order Tylor expansion of the exponential term in equation (9) we can derive equation (10) . Then with a bit of algebra we can rearrange equation (10) into (11) to estimate the value of R_CC_{BWC}. $t0(K)$ can also be estimated using equation (12). Unfortunately there is still one unknown in equation (11) $\frac{V_t}{A_v}$, but it can be determined using two different ramp slopes and equating the time constant as shown in equation (13). Simplifying (13) we find a quadratic equation in $\frac{V_t}{A_v}$ as shown in equation (14) . Therefore using two measured, or in the case of this paper simulated, delay times with different ramp slopes we can estimate the time constant and the switching voltage divided by the trans-conductance amplifier gain, i.e. $\widehat{R_CC_{BWC}}$ and $\frac{\widehat{V_t}}{A_v}$.

$$V_t = KA_v(t0(K) + \frac{V_t}{A_vK} + R_CC_{BWC}\left(e^{-\frac{(t0(K)+V_t/(A_vK))}{R_CC_{BWC}}} - 1\right) \quad (9)$$

$$V_t = KA_v\left(t0 + \frac{V_t}{A_vK} + R_CC_{BWC}\left(\begin{array}{l}1+\left(\frac{-(t0+V_t/(A_vK))}{R_CC_{BWC}}\right)+\\ \frac{1}{2!}\left(\frac{-(t0+V_t/(A_vK))}{R_CC_{BWC}}\right)^2+\\ O\left(\frac{-(t0+V_t/(A_vK))}{R_CC_{BWC}}\right)^3-1\end{array}\right)\right) \quad (10)$$

$$\approx KA_v\frac{(t0+V_t/(A_vK))^2}{2R_CC_{BWC}}$$

$$R_cC_{BWC} \approx A_v\frac{(t0(K)+V_t/(A_vK))^2K}{2V_t} = A_v\frac{\left(t0(K)^2+2t0(K)\left(\frac{V_t}{A_vK}\right)+\left(\frac{V_t}{A_vK}\right)^2\right)K}{2V_t} \quad (11)$$

$$t0(K) \approx \sqrt{\frac{2V_tC_{BWC}}{Kg_{m,CP}}} - \frac{V_t}{A_vK} \quad (12)$$

$$\left(t0(K_1)^2+2t0(K_1)\left(\frac{V_t}{A_vK_1}\right)+\left(\frac{V_t}{A_vK_1}\right)^2\right)K_1 = \left(t0(K_2)^2+2t0(K_2)\left(\frac{V_t}{A_vK_2}\right)+\left(\frac{V_t}{A_vK_2}\right)^2\right)K_2 \quad (13)$$

$$t0(K_2)^2K_2 - t0(K_1)^2K_1 + 2(t0(K_2) - t0(K_1))\left(\frac{V_t}{A_v}\right)+\left(\frac{1}{K_2}-\frac{1}{K_1}\right)\left(\frac{V_t}{A_v}\right)^2 = 0 \quad (14)$$

To determine the lower bound on the input referred comparator noise we also need to estimate the band limiting capacitance C_{BWC}. We can get a rough estimate by rearranging equation (10) to (15). Then assuming the comparator bias can be operated in subthreshold $g_{m,CP} = \frac{i_d\kappa}{v_{th}}$. Note that i_d is the drain current in the differential pair transistors, κ is the subthreshold gate efficiency factor and $v_{th} = \frac{kT}{q}$ is the thermal voltage. κ can be determined from the SPICE model for the process.

If the comparator is designed such that the source and bulk of MP3 (AVDD2) can be lowered below AVDD then we can directly estimate V_t using equation (16), where ΔV_{source} is the change in source and bulk voltage of MP3.

$$C_{BWC}V_t \approx \frac{\left(t0+\frac{V_t}{A_vK}\right)^2Kg_{m,CP}}{2} \quad (15)$$

$$V_t = \frac{\Delta V_{source}}{\frac{C_{BWC}(V_t+\Delta V_{source})}{C_{BWC}(V_t)}-1} \quad (16)$$

IV. Results

We validate our model using SPICE simulations in this Section. Using the circuit shown in Figure 1 with the devices sizes and biases given in Table 1 we measure delay times in SPICE using $K = \{50.2, 12.5\}kV/sec$ and $AVDD2 = \{AVDD, AVDD - 0.2\}V$. Table 2 shows the estimated parameters based on the simulated measurements. Note that the SPICE models used for simulation are from a TSMC 22nm process. Tables 3 and 4 show a delay time comparison between the model and SPICE simulation. Using the same parameters, we compare the accuracy of the noise model to SPICE transient noise analysis shown in Table 5. Only white noise sources are included in the SPICE noise analysis with 256 Monte Carlo simulations.

Device	Parameter (unit)	Value
MN1	W/L (um)	2.5/0.5
MN2	W/L (um)	2.5/0.5
MN3	W/L (um)	12/1.8
MP4	W/L (um)	12/1.8
MP5	W/L (um)	1.25/0.5
MP1	W/L (um)	2.5/1.8
MP2	W/L (um)	2.5/1.8
MP3	W/L (um)	2.5/1.8
C_L	(fF)	70
I_{bias}	(nA)	1000

Table 1:SPICE circuit parameters

Parameter	Unit	Value
V_t/A_v	V	0.00148
R_CC_{BWC}	usec	2.83
V_t	V	0.6
C_{BWC}	fF	98.2
$g_{m,CP}$	uS	14

Table 2: Estimated model parameters

Parameter	Units	Values ($C_L = 70\,fF$)				
K	kV/s	33.4	25	20	16.6	14.3
SPICE $t0$	usec	0.456	0.518	0.572	6.20	0.663
Model $t0$	usec	0.456	0.518	0.572	6.20	0.663
Error	%	<0.1	<0.1	<0.1	<0.1	<0.1

Table 3: Comparator delay as a function of ramp slope

Parameter	Units	Values ($K = 20kV/\sec$)		
C_L (fF)	fF	35	70	100
SPICE $t0$	usec	0.421	0.572	0.680
Model $t0$	usec	0.444	0.572	0.665
Error	%	5.6	<0.1	2.2

Table 4: Comparator delay as a function load capacitance

Parameter	Units	Values ($K = 20kV/\sec$)		
C_L (fF)	fF	35	70	100
SPICE $\sigma_{V_{diff}}(t0)$	uV RMS	43	37	36
Model $\sigma_{V_{diff}}(t0)$	uV RMS	48.8	43	39.5
Error	%	13	16	10

Table 5: Input-referred comparator noise

V. Discussion

In this model we have assumed that the trans-conductance $g_{m,CP}$, the output resistance R_C and the bandwidth control capacitance C_{BWC} are all constants. This is not true, they are all time vary during the switching operation of the comparator. The trans-conductance changes due to the current switching between MN3 and MN4, the output resistance changes due to the large drain to source voltage swing on MP2 and the bandwidth limiting capacitance changes due the Miller Effect of MP3. This limits the accuracy of the model and makes the estimated parameters a time weighted average over the switching period.

Although our simplified model does not capture all of the dynamics of the comparator, it does allows us to estimate delay times with less than 10% error and input referred white noise with less than 20% error.

VI. Conclusions

We have extended a previously published comparator model to enable parameter estimation from measured data. Using estimated model parameters we have shown that this methodology can be used to roughly determine the delay time and the noise floor of the comparators used in standard single slope column parallel ADCs. We have also shown the relative model error in regards to variations in the ramp slope and band limiting capacitance.

References

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[4] https://en.wikipedia.org/wiki/It%C3%B4_calculus

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